**Low power cam design using 9T SRAM cell**

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# Abstract

Large-capacity content addressable memory (CAM) is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of application that require high-speed table lookup. The main CAM-design challenge is to reduce power consumption associated with the large amount of parallel active circuitry, without sacrificing speed or memory density [1].

# Introduction

STATE-OF-THE-ART DSP cores and advanced healthcaressoCs, benefit from availability of on-chip SRAMs with substantially reduced power dissipation and improved energy efficiency. Integrated SRAMs play a crucial role in providing the required density, performance, power, and energy consumption of applications. By aggressively scaling supply voltage near or below transistor's threshold voltage, power and energy efficiency of SRAMs can be greatly ameliorated at the expense of performance. However, the vulnerability of SRAMs to PVT fluctuations makes reliable near- and sub-threshold operations extremely challenging in deep sub-micrometer CMOS technologies. Simultaneously, other design metrics such as stability, read/write margin, and leakage need to be carefully revisited for the reliable operation [6].

The CAM is designed from the SRAM and XOR. Since, the Static Random-Access Memory (SRAM) is a type of semiconductor volatile memory (RAM) which keeps its data until the power is turns OFF. SRAM will store the binary logic bits ‘1’ or ‘0’. It contains of an array of memory cells along with the row and column circuitry. SRAM has design to fill needs that are to provide direct interface with CPU at speeds not achievable by DRAMs and to replace DRAMs in systems that require very low power consumption. The basic architecture of a static RAM includes one or more rectangular arrays of memory cells with support circuitry to decode addresses, and implement the required read and write operations. SRAM memory arrays are arranged in rows and columns of memory cells called word-lines and bit-lines respectively. In SRAM, the word-lines are made from polysilicon while the bit-lines are metal [2]. There are different ways to implement the SRAM. Since, we can build the SRAM using 6T, 8T, 9T... etc. In this paper, we provide a brief description about a low power CAM design using 9T SRAM cell and compare our result with other results that are using 6T SRAM.

# Problem statement

Part A: The Ideal [1]

The ideal concept for content address memory is a storage device that stores data in its memory cell SRAM. But additionally, it also has a comparison circuitry which is used to compare search data with the data contents stored in its memory simultaneously. This comparison circuitry in the CAM cell occupies extra area than usual memory cell.

We have many processes of reading, writing and comparison. Both the reading and writing process are built and represented in the usual RAM. So, this little storage uses a simple SRAM cell that contains two reflective crosses that form positive reactions as a latch extension. Finally, the comparison is constructed using the logical gate XOR. It is unique in cam.

Part B: The Reality

In fact, a CAM cell in various ways to build it is costly because it occupies extra area than usual memory cell. Hence there is more power dissipation but high speed due to parallel searching operation.

The current design use 6t SRAM and XOR gate with 8 transistors to compare content of SRAM with CAM data cell. This design consumes more power dissipation because we use 6t SRAM and consumes extra area because using 8t XOR gate.

**Part C:**The **consequences**

The method that we used and applied to reduce energy significantly and on the other hand reduce the space used. We have made two changes:

The first: We use 9t SRAM instead of 6t SRAM, and one of its most important advantages is its consumption with low voltage, which has the greatest impact on reducing energy consumption, but if you look at a time side, we conclude that these leads to an increase in time and also note an increase in the region but can Increase fade in the area by improving the second method. The time, on the philosophical side, of the way CAM works gives very fast results compared to other methods so it is able to withstand this damage.

Secondly, we improved the XOR gate as we built it using the pass gate of 4 transistors. Which greatly improves the area for all cam cell.

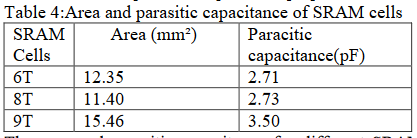
# Background and compression to other systems [3]

Part A SRAM:

1- The area and parasitic capacitance:

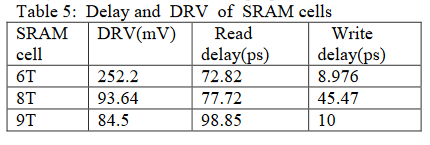
The area and parasitic capacitance for different SRAM cell is given above. The write power is high in 9T is because of high parasitic capacitance.

Table 1:Area and parasitic capacitance of SRAM cells [3]



2- Delay and data retention voltage Simulation results for data retention read delay and write delay is shown in Table 2 below.

Table 2: Delay and DRV of SRAM cells

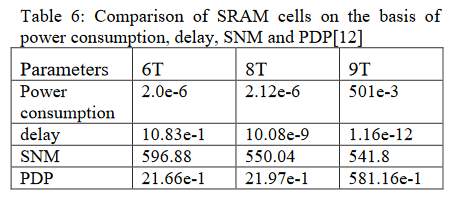


Read delay is highest for 9T SRAM cell because high-Vt transistors are used in it, due to which the driving capability of the transistor reduces. Due to the single bit line in 8T SRAM cell its write delay is higher as compared to another SRAM cell.

3- Active power consumption

The tri-Vt7T memory array consumes the lowest write power. The single write bit line of a 7T SRAM cell is maintained at VDD or V GND following a write operation. The write bit line is not necessarily charged or discharged prior to each write operation if the incoming data is identical with the initial state of the write bit line. Alternatively, one of the two-bit lines is discharged prior to a write operation regardless of the incoming data in an 8T or 9T SRAM cell. The tri-Vt 8T SRAM array consumes the lowest read power. Alternatively, the tri-Vt7T SRAM array suffers from the highest read power consumption due to the highest read bit line capacitance and bit line voltage drop.

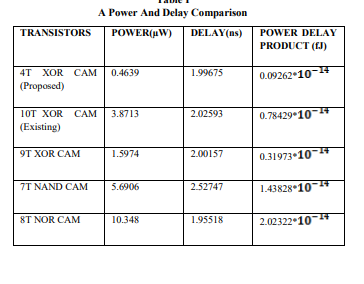
Table 3: Comparison of SRAM cells on the basis of power consumption, delay



Part B CAM match [7]:

In table for we show a comparison for different cam cell power and delay for different compare gates.

Table 4:A Power And Delay Comparison



From the table 4 it shows that 4T XOR CAM cell consumes less power and delay when compared to other CAM cell transistor levels. A XOR CAM Cell 4T have been designed in this paper. The various design of CAM Cell and proposed XOR CAM. Further the energy (power-delay product) saved through this circuit is more when compared to the Existing circuit has shown in the table. Therefore, the proposed design can be use in low power application of CAM and also in CAM architectures such as Hybrid, Banked and Gated ML sensing technique.

# Proposed system, simulation result and methodology

A. Proposed 9T SRAM Cell [4]

The proposed 9T SRAM cell is shown in figure 1 and its layout in figure 2. The read port comprises three NMOS transistors for realizing equalized bit line leakage and improving bit line sensing margin in a single-ended read bit line (RBL).

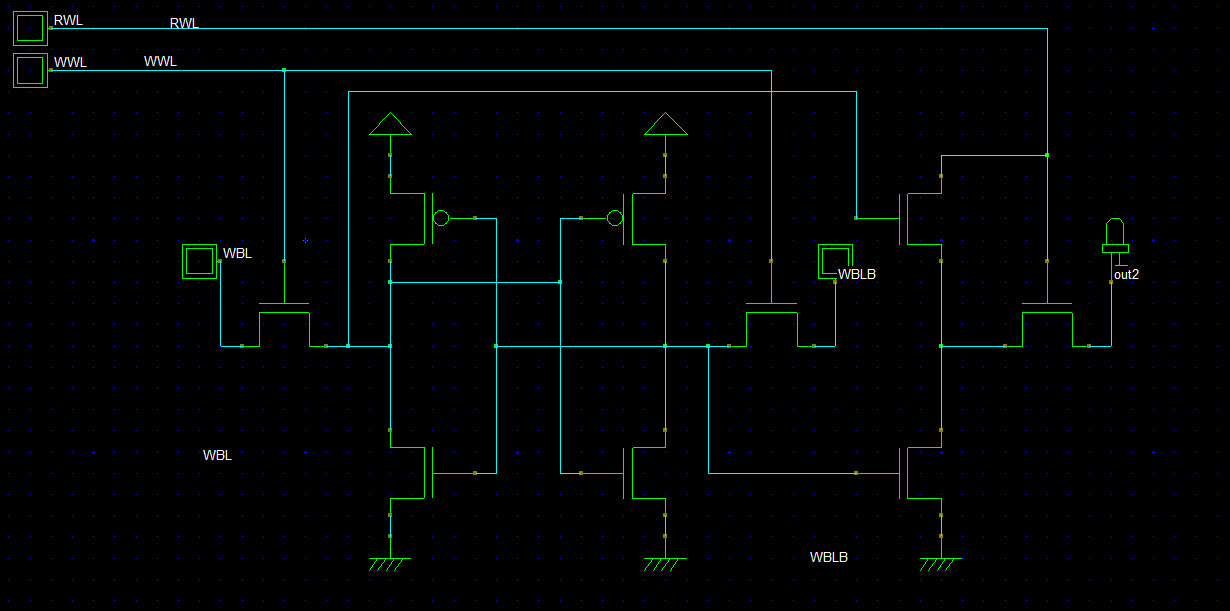


Figure :9t SRAM cell

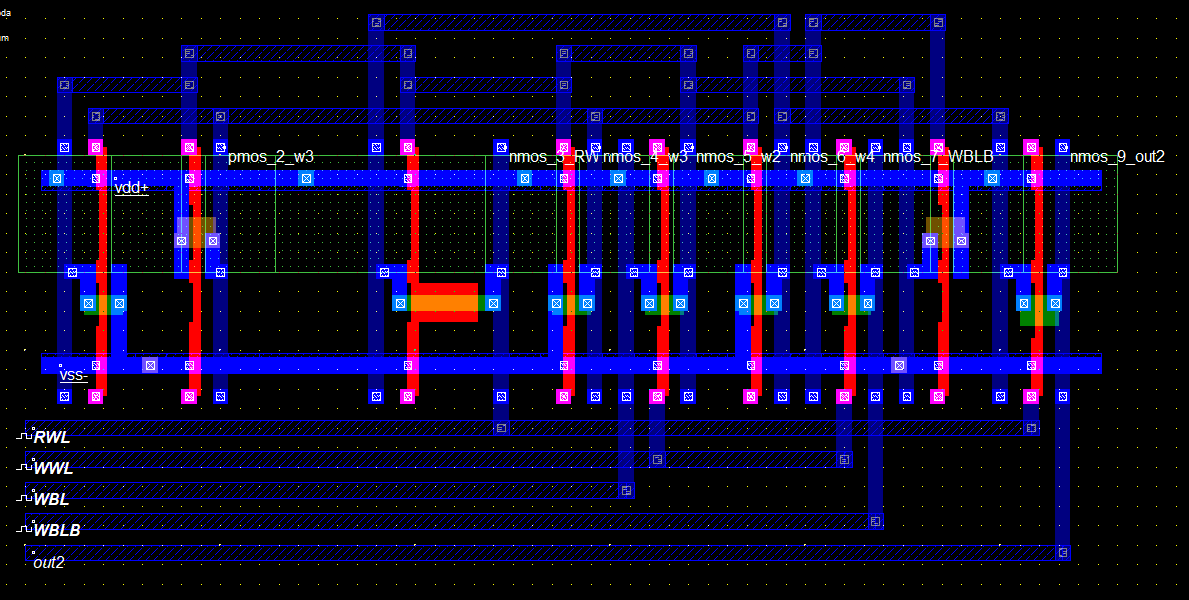


Figure :9t SRAM layout

The write access paths and the data storage latch are implemented with HVT devices for leakage reduction while the read port employs LVT devices for performance. In figure 3 we show the layout area of the 9T cell occupies an area of 142.1um2 based on logic design rules. A write operation is enabled by activating a write word line (WWL) and completed when the data loaded at WBL and WBLB is written into Q and QB.

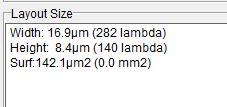


Figure 3:9t SRAM area

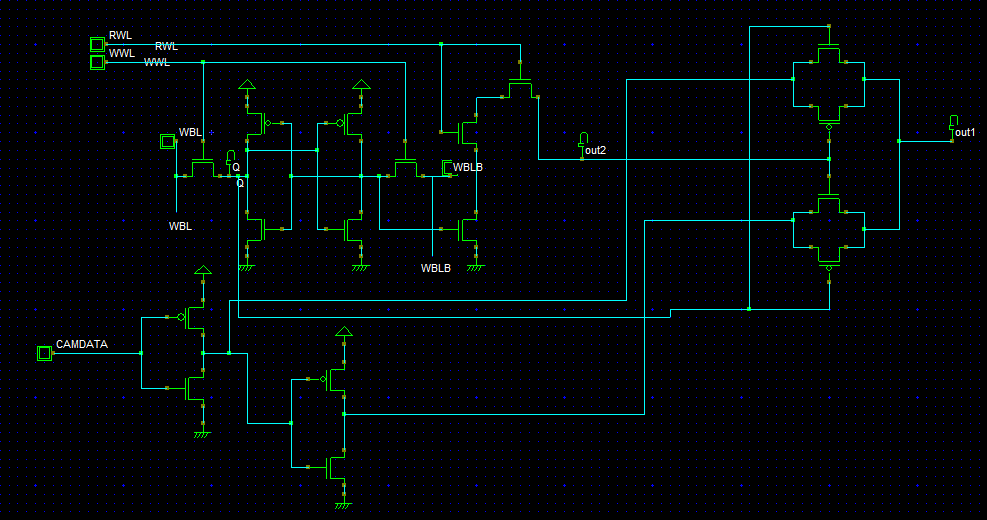
B. Proposed cam-cell circuit design [5]

Figure :Proposed cam cell schematic

The proposed CAM cell circuit shown in figure 4. If you focus on the proposed system you will see the compare circuit includes circuitry which is controlled by the logic values of single-ended inverted reference bit cam data and the complementary stored bits BIT, BITX, which forms the inputs of the desired compare-circuit. The output of the compare-circuit is a match-bit which indicates whether the reference bit cam data matches the stored bit BIT.

The compare-circuit output a match-bit with logic value 1 when the reference bit CAMDATA differs from the stored bit BIT. And logic value 0 when the reference bit CAMDATA matches the stored bit BIT. During write operation to CAM cell, bits BIT, and BITX are written into the bit-cell. To perform a CAM compare operation, i.e., to determine whether reference bit CD matches the stored bit BIT and therefor assert output as a result of that compare, first the reference bit CD is asserted, and then the compare-circuit determines whether the stored bit BIT matches reference bit CD stored BIT, and stored complementary bit BITX, which control pass circuit, pull-up circuit and pull-down circuit. If the logic level of CD matches the logic level of BIT, then the compare circuit produces match-bit at a first logic level (=1).

In figure 5 we show an example of a 1-bit block/circuit diagram regarding the proposed implementation of CAM system including. Then using this block, we build multiple CAM cells (8-bit CAM cell) that share compare circuitry shown in figure 6. Each of the CAM cells in the diagram includes a portion of compare-circuit locally to one cell and repeated for each of the CAM cells.

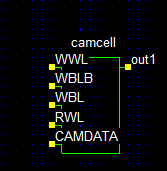


Figure :CAM cell 1-bit block

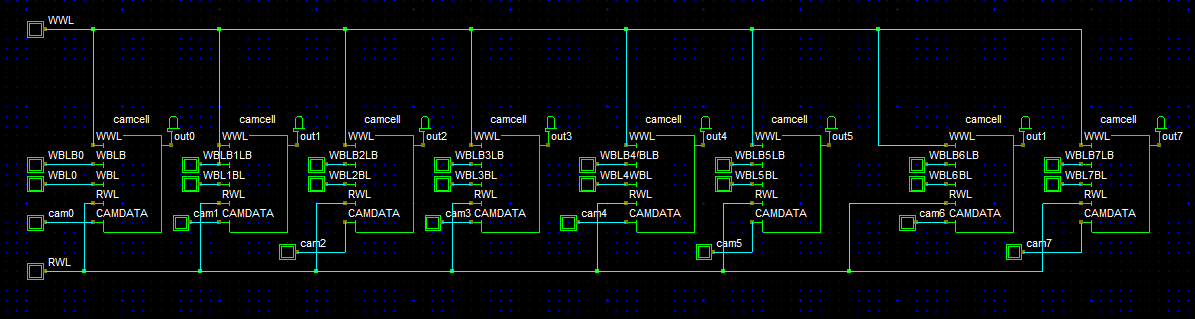


Figure :8-bit CAM cell

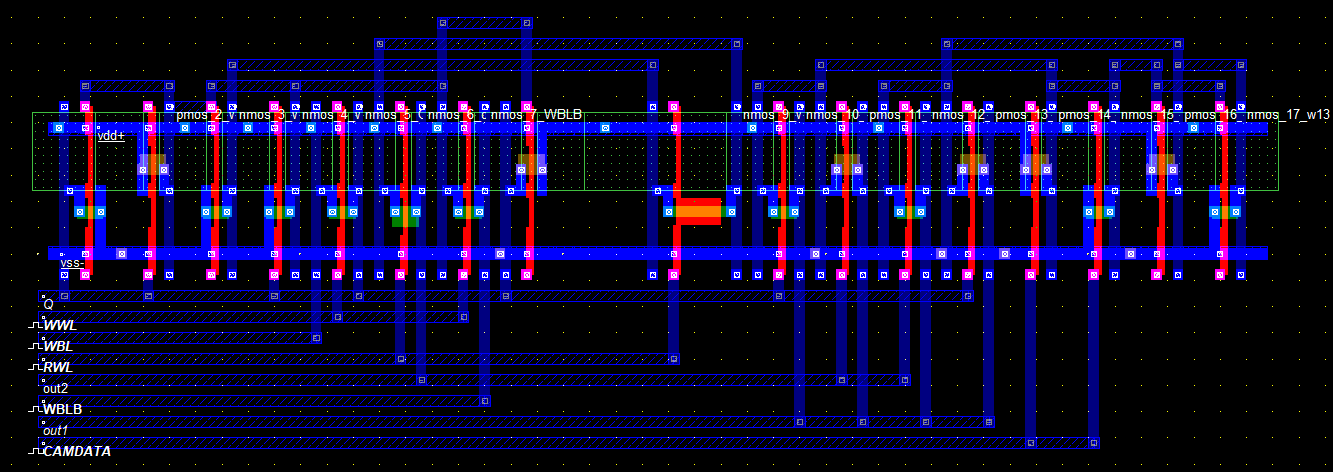
C. Simulation and results

Figure :Layout for 1bit cam cell

In figure 7 we show the layout for 1bit cam cell that we proposed and show in figure 4. The proposed design is implemented and simulated using DSCH3 and Microwind under 45nm process environment.

The area for CAM cell layout was 279.8µm2

In figure 8 we show the simulation result for 1bit cam cell that we proposed and show in figure 4.

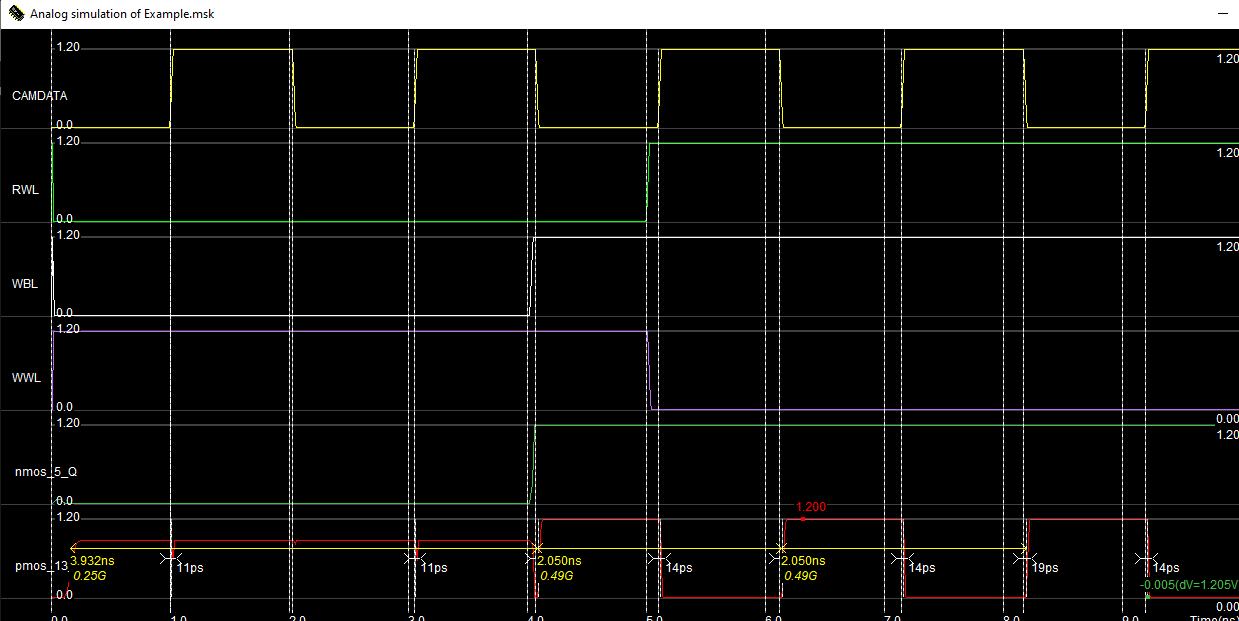


Figure :My Simulation for 1-bit CAM cell

As the figure 8 above, that we initially did the writing on CAM when write enable logic 1 (WWL) and store data in 9t SRAM cell. Then we were read the stored data (Q in simulation) by make read enable (RWL) on. After that we compare this data with CAMDATA input and the result as you see in same figure (out). Power dissipation was 77.1 micro watt.

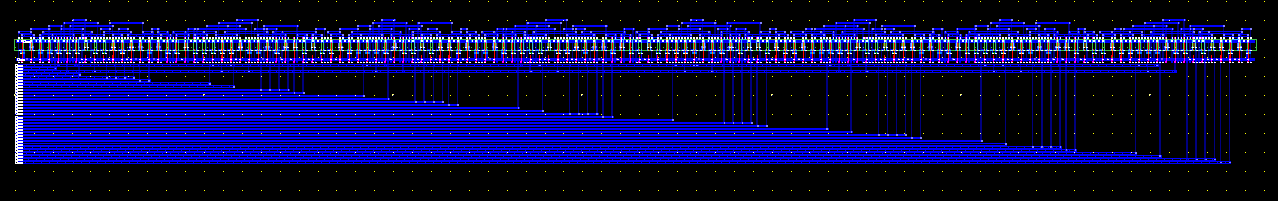
In figure 9 we show the layout for 8-bit cam cell that we proposed and show in figure 6.

Figure :Layout for 8-bit cam cell

In figure 10 below we show the area for 8-bit cam cell

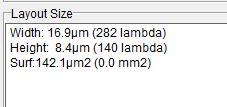


Figure 10:area for 8-bit cam cell

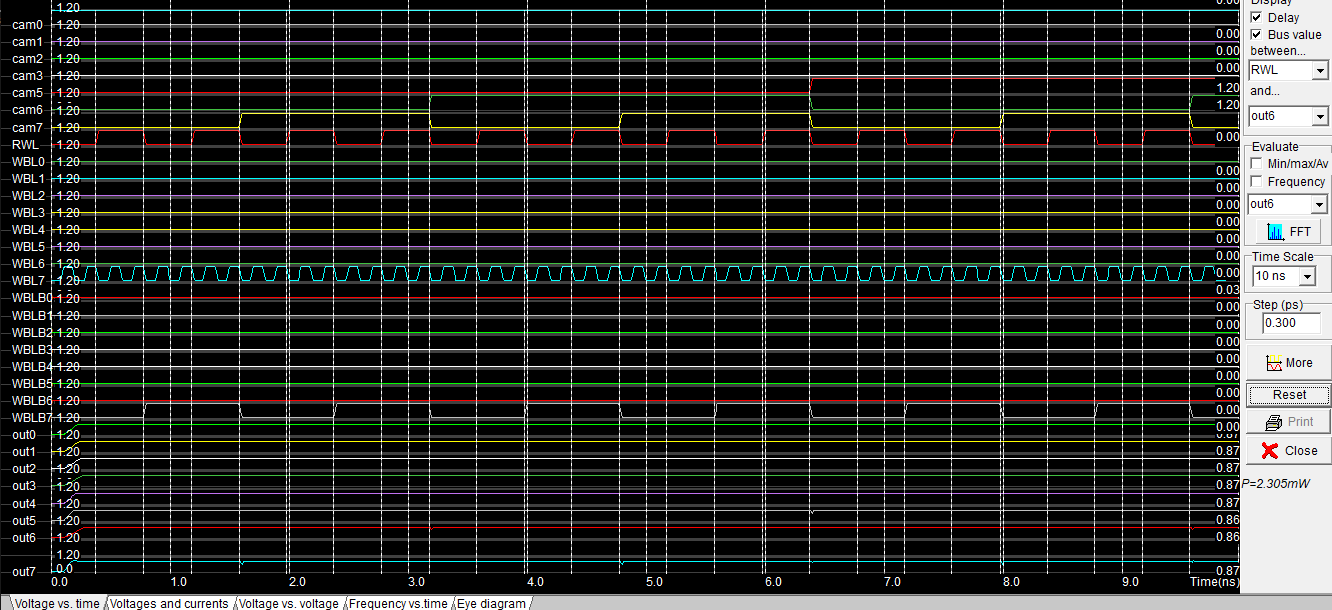


Figure :Simulation for 80bit cam cell

In figure 11 above, we show the simulation result and test for 8-bit CAM cell hat we the procedure for understand this result is same as 1-bit CAM cell simulation but now for 8 block of 1-bit so we write in 8 SRAM when write enable logic 1 (WWL) and store data in 9t SRAM cell. Then we were read from 8 SRAM the stored data (Q in simulation) by make read enable (RWL) on. After that we compare this data for each cam cell with CAMDATA input and the result as you see in same figure (out0-out7). Power dissipation was 2.305mwatt.

# Conclusion

This paper presents proposal circuit technique to implement A Content Addressable Memory (CAM). CAM system includes CAM cells, each having a compare-circuit and a memory bit-cell that stores complementary bits. Memory is energy efficient 9t SRAM with reliable read operation under ultra-low voltage. Leakage and energy efficiency are primary concerns for ultra-low voltage SRAM design. CAM is a memory unit that performs content matching instead of address decoding. This proposed implementation avoids produces crowbar current during bit-cell write operation since there is one gate delay between BIT and BITX which opens one pass gate before closing the second. Sharing resources across all cells reduces the total device width. The new implementation outperforms the conventional CAM cell implementation in terms of current saving with increase performance impact in terms of area and power.

# VI. References

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